HACETTEPE UNIVERSITY
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
ELE-314 ELECTRONICS LABORATORY III

EXPERIMENT 3
RTL AND DTL LOGIC GATES

1. PURPOSE : To design the RTL "NOR" and DTL "NAND" logic gates.

2. THEORY : The procedure while designing the RTL and DTL logic gates could be summarized as follows:
Initially determine the cut-off condition of the transistor and by considering the transfer characteristics of the circuit to be realized, find a relation (inequality) between the resistors. Then consider the saturation condition of the transistor. Here there exists three possible situations which are the no load condition, the cut-off or the saturation state of the stage connected as a load. The design should be held at the Worst Case Conditions (WCC). In RTL circuits the worst case of the loading is the saturation condition of the N gates connected to the output. Considering the saturation condition of the transistor, another inequality between resistors is obtained and the appropriate values are chosen by use of these two inequalities. In DTL circuits this is the cut-off condition of the N stages connected to the output. In DTL circuits, the loading condition should be taken into account.

Use the following procedure to design the RTL NOR gate in Figure 2:

1. For the transistor at saturation, consider:

(a) The condition $I_{CSAT} \leq I_{CMAX}$ and find an inequality for R_L.

(b) The condition $\beta I_{BSAT} \geq I_{CSAT}$ and find an inequality for R_2 when only one input is greater than or equal to V_{IHmin}.

2. For the transistor at cut-off, let all inputs are less than or equal to V_{ILmax} and consider:

(a) The condition on the base-emitter junction and find a relation between R_1 and R_2.

(b) The minimum output voltage V_{Omin} with N loads connected to the output and find a relation between $R_1$and R_L.

3. Choose appropriate values for R_L due to 1(a);R_1 due to 2(b);R_2 due to1(b) and 2(a).

Use the following procedure to design the DTL NAND gate in Figure 4:

1. Find an inequality for the cut-off condition between resistors R_2 and R_3 when only one input is less than or equal to V_{ILmax}.

2. For the no load saturation condition, find another inequality between R_2 and R_3 when all inputs are greater than or equal to V_{IHmin} (Consider I_{CSAT} for I_{CMAX} satisfying $I_{CSAT} \leq I_{CMAX}$).

3. For the no load saturation condition, find an inequality between R_2 and R_1 considering that the diodes should be ON when all inputs are greater than or equal to V_{IHmin} .

4. With N loads connected to the output and the transistor is at saturation, find an inequality between R_1 and R_L.

5. Choose appropriate values for R_1 due to (4), R_2 due to (3); R_3 due to (1) and (2). Choose an appropriate value for R_1 by assuming $R_2 + R_3 >> R_1$

NOISE MARGIN: After determining the transfer function under WCC, DC noise margin is given by (Refer to Figure 1.)

$V_{NMH} = V_{OHmin} - V_{IHmin}$

$V_{NML} = V_{ILmax} - V_{OLmax}$

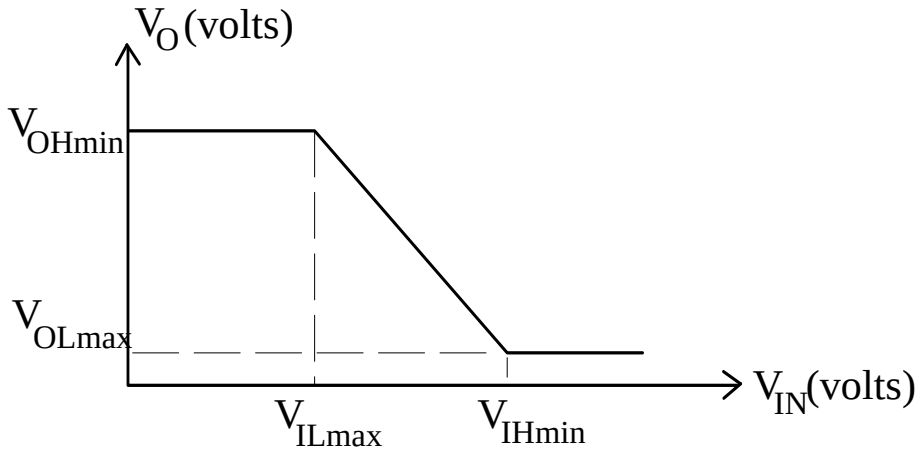


Figure 1 Transfer characteristics under WCC.

Also note the following terms:

Logic swing: $LS = V_{OHmin} - V_{OLmax}$

I_{CCH}: The amount of current drawn from the supply V_{CC} when the output of the gate is at HIGH state.

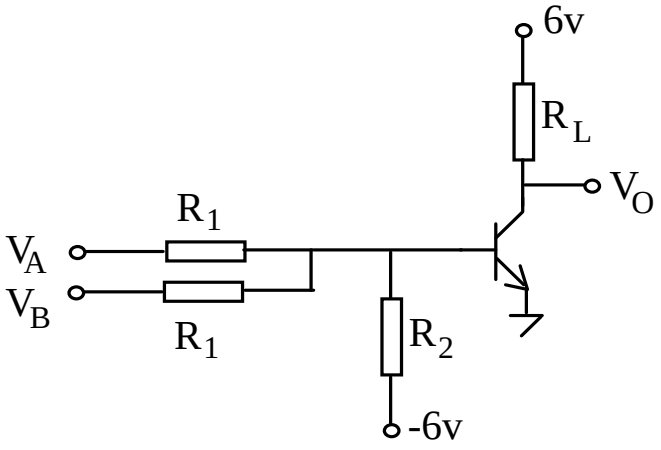
I_{CCL}: The amount of current drawn from the supply V_{CC} when the output of the gate is at LOW state.

Average power dissipation per gate: $P_{D(avg)} = V_{CC} [I_{CCH} + I_{CCL}] / 2$ (in mWatts)

Propagation delay time: $t_P = (t_{PHL}+t_{PLH}) / 2$ (in ns),
where t_{PHL} is the delay when the output switches from HIGH state to LOW state and t_{PLH} is the delay from LOW state to HIGH state.
Power delay product: $PDP = P_{D(avg)} \times t_P$ (in pJ)

1. PRELIMINARY WORK:

3.1 Refer to Figure 2 and design a two input positive logic RTL NOR gate due to the following specifications (choose the resistor values from the component list given at the end of preliminary work):



$\beta_N = 125$
$V_D = 0.6V$
$V_{BEON} = 0.5V$
$V_{BESAT} = 0.7V$
$V_{CESAT} = 0.2V$

Figure 2 RTL NOR Gate.

a. Maximum collector current $I_{CMAX} = 10$ mA.
b. Fan-out N = 4.
c. Minimum collector voltage under WWC when the BJT is in CUT-OFF, is 3.7 volts.
d. When one of the inputs is zero ($V_B = 0$), the transfer function for no load is shown in Figure 3.

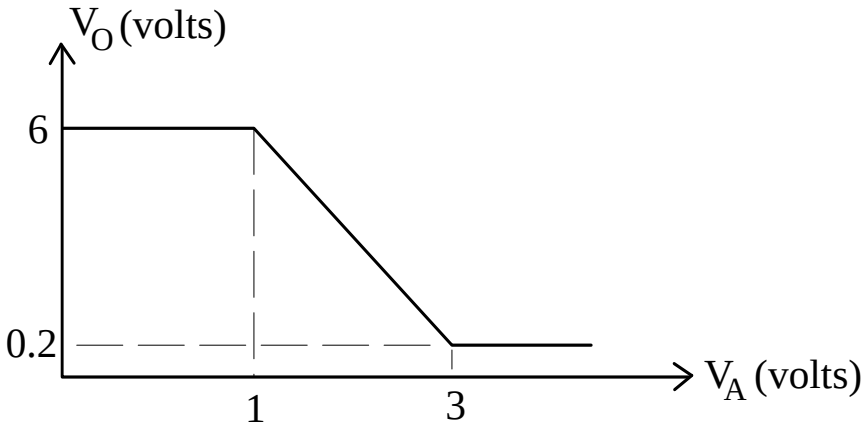


Figure 3 Transfer characteristics under WCC.

3.2. Obtain the transfer characteristic of NOR gate you designed with no load for V_B = 0V and $V_B = V_A$.

3.3. Obtain the transfer characteristic of NOR gate you designed with load for V_B = 0V and $V_B = V_A$. Find an equivalent circuit to simulate load that is realizing the output current as if 4 input stages of NOR gate are connected to the output of the previous gate.

3.4 Refer to Figure 4 and design a two input positive logic DTL NAND gate due to the following specifications (choose the resistor values from the component list given at the end of the experiment):

a. R_L = 1.5 KΩ and maximum collector current I_{CMAX} = 10 mA.

b. Fan-out N = 4.

c. The transfer function under WCC (V_B = 6 volts or equivalently V_B is open circuit), is shown in Figure 3.

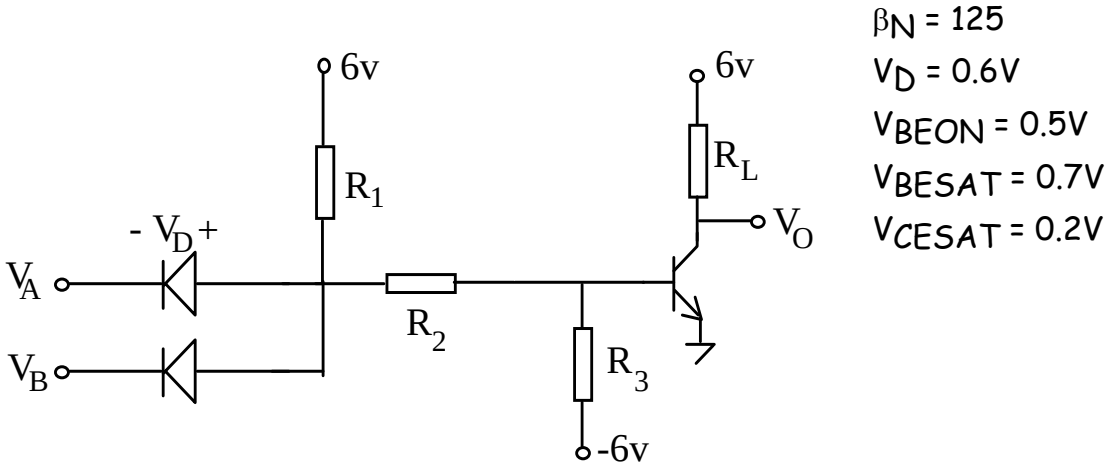


Figure 4 DTL NAND Gate.

(P.S. Choose the standart values for resistors from the component list.)

3.5. Obtain the transfer characteristic of NAND gate you designed with no load for V_B = open.

3.6. Obtain the transfer characteristic of NAND gate you designed with load for V_B = open. Find an equivalent circuit to simulate load that is realizing the output current as if 4 input stages of NAND gate are connected to the output of the previous gate.

3.7 Obtain the results of step 3.2, 3.3, 3.5 and 3.6 by simulating related circuits in Pspice. Compare the results of simulations with the theoretical ones.

4. COMPONENT AND EQUIPMENT LIST:

Oscilloscope	#1	BC 107	#1	4.7 KΩ	#1	1.5 KΩ	#1
Power Supply	#1	1N 4001	#3	22 KΩ	#1	1 KΩ	#1
AVO	#1	3.9 KΩ	#2	680 Ω	#1		

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